Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 1, 17, 84, 93, 104 and 107 as follows:

Listing of Claims:

1. (Currently Amended) In a memory system having a memory hub controller and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, a method of coupling command, address and data signals between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a first communications path having a first plurality of signal lines;

coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a second communications path having a second plurality of signal lines, where the sum of the first plurality of signal lines and the second plurality of signal lines is a fixed value; and

altering the first ~~capacity~~plurality of signal lines and the second ~~capacity~~plurality of signal lines by transitioning at least one of the first plurality of signal lines from the first communications path to the second communications path or transitioning at least one of the second plurality of signal lines from the second communications path to the first communications path during the operation of the memory system based on the rate at which the signals are being coupled from the memory hub controller to the memory hub in the at least one memory module and based on the rate at which the signals are being coupled from the memory hub in the at least one memory module to the memory hub controller.

2. (Canceled)

3. (Previously Presented) The method of claim 1 wherein the acts of altering the first capacity and the second capacity comprise:

at the memory hub controller, determining the rate at which the signals are being coupled between the memory hub controller and the memory hub in the at least one memory module; and

altering the first capacity and the second capacity based on the determined rate at which the signals are being coupled between the memory hub controller and the memory hub in the at least one memory module.

4. (Previously Presented) The method of claim 1 wherein the acts of altering the first capacity and the second capacity comprise:

at the memory hub of the at least one memory module, determining the rate at which the signals are being coupled between the memory hub controller and the memory hub; and

altering the first capacity and the second capacity based on the determined rate at which the signals are being coupled between the memory hub controller and the memory hub.

5. (Previously Presented) The method of claim 1 wherein the acts of altering the first capacity and the second capacity comprise:

using software on a computer readable medium to determine the rate at which the signals are being coupled between the memory hub controller and the memory hub of the at least one memory module; and

altering the first capacity and the second capacity based on the rate determined by the software on a computer readable medium.

6. (Previously Presented) The method of claim 5 wherein the act of using software on a computer readable medium to determine the rate at which the signals are being coupled between the memory hub controller and the memory hub of the at least one memory

module comprises using operating system software on a computer readable medium to determine the rate at which the signals are being coupled between the memory hub controller and the memory hub of the at least one memory module.

7. (Previously Presented) The method of claim 1 wherein the acts of altering the first capacity and the second capacity comprise:

determining the rate at which the signals are being coupled between the memory hub controller and the memory hub of the at least one memory module at a location other than the memory hub of the at least one memory module;

transmitting information indicative of the determined rate to the memory hub of the at least one memory module; and

altering the first capacity and the second capacity based on the transmitted information.

8. (Previously Presented) The method of claim 1 wherein the acts of altering the first capacity and the second capacity comprise:

determining the rate at which the signals are being coupled between the memory hub controller and the memory hub of the at least one memory module at a location other than the memory hub controller;

transmitting information indicative of the determined rate to the memory hub controller; and

altering the first capacity and the second capacity based on the transmitted information.

9. (Original) The method of claim 1 wherein the acts of altering the first capacity and the second capacity during the operation of the memory system comprise configuring buffers in the memory hub controller and in the memory hub of the at least one memory module as either input buffers or output buffers.

10. (Original) The method of claim 1 wherein the acts of altering the first capacity and the second capacity comprise altering the first capacity and the second capacity based on the rate at which it is anticipated that the signals will be coupled from the memory hub controller to the memory hub in the at least one memory module and based on the rate at which it is anticipated that the signals will be coupled from the memory hub in the at least one memory module to the module memory hub controller.

11. (Original) The method of claim 10 wherein the acts of altering the first capacity and the second capacity comprise:

determining the rate at which it is anticipated that the signals will be coupled between the memory hub controller and the memory hub in the at least one memory module based on the type of hardware included in a system associated with the memory system; and

altering the first capacity and the second capacity based on the determined rate at which it is anticipated that the signals will be coupled between the memory hub controller and the memory hub in the at least one memory module.

12. (Previously Presented) The method of claim 1 wherein the acts of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity within a range of minimum and maximum values for the first capacity and the second capacity respectively.

13.-14. (Canceled)

15. (Previously Presented) The method of claim 1 wherein the act of coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module comprises transmitting a packet containing command, address and data signals from the memory hub controller to the memory hub in the at least one memory module.

16. (Original) The method of claim 1 wherein the acts of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity during the initialization of the memory system.

17. (Currently Amended) In a memory system having a memory hub controller, at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, and a bus having [[a]] M signal lines coupled between the memory hub controller and the memory hub in the at least one memory module, a method of coupling command, address and data signals through the bus between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

coupling command, address and data signals in a downstream direction from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus;

coupling data signals in [[a]]an upstream direction from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus, where N+P = M; ~~and~~

determining a first rate at which data signals are being coupled from the memory hub in the at least one memory module to the memory hub controller;

determining a second rate at which command, address and data signals are being coupled from the memory hub controller to the memory hub in the at least one memory module; and

altering the values of N and P during the operation of the memory system based on the first and second rates such that at least one of the signal lines of the bus transitions from coupling in the upstream direction to coupling in the downstream direction or from coupling in the downstream direction to coupling in the upstream direction.

18. (Canceled)

19. (Previously Presented) The method of claim 17 wherein the acts of determining the first rate and determining the second rate comprise determining the first and second rates at the memory hub controller.

20. (Previously Presented) The method of claim 17 wherein the acts of determining the first rate and determining the second rate comprise determining the first and second rates at the memory hub.

21. (Previously Presented) The method of claim 17 wherein the acts of altering the values of N and P comprise:

using software on a computer readable medium to determine the rate at which the signals are being coupled through the bus; and

altering the values of N and P based on the rate determined by the software on a computer readable medium.

22. (Previously Presented) The method of claim 21 wherein the act of using software on a computer readable medium to determine the rate at which the signals are being coupled through the bus comprises using operating system software on a computer readable medium to determine the rate at which the signals are being coupled through the bus.

23. (Previously Presented) The method of claim 17 wherein the acts of altering the values of N and P based on the rate at which the signals are being coupled through the bus comprise altering the values of N and P based on the rate at which the signals are being coupled through the bus from the memory hub controller to the memory hub in the at least one memory module.

24. (Previously Presented) The method of claim 17 wherein the acts of altering the values of N and P based on the rate at which the signals are being coupled through the bus comprise altering the values of N and P based on the rate at which the signals are being coupled through the bus from the memory hub in the at least one memory module to the memory hub controller.

25. (Previously Presented) The method of claim 17 wherein the acts of altering the values of N and P comprise:

determining the rate at which the signals are being coupled through the bus at a location other than the memory hub of the at least one memory module;

transmitting information indicative of the determined rate to the memory hub of the at least one memory module; and

altering the altering the values of N and P based on the transmitted information.

26. (Previously Presented) The method of claim 17 wherein the acts of altering the values of N and P comprise:

determining the rate at which the signals are being coupled through the bus at a location other than the memory hub controller;

transmitting information indicative of the determined rate to the memory hub controller; and

altering the altering the values of N and P based on the transmitted information.

27. (Original) The method of claim 17 wherein the acts of altering the values of N and P during the operation of the memory system comprise configuring buffers in the memory hub controller and in the memory hub of the at least one memory module as either input buffers or output buffers.

28. (Previously Presented) The method of claim 17 wherein the acts of altering the values of N and P comprise altering the altering the values of N and P based on the rate at which it is anticipated that the signals will be coupled through the bus.

29. (Original) The method of claim 28 wherein the acts of altering the values of N and P comprise:

determining the rate at which it is anticipated that the signals will be coupled through the bus; and

altering the values of N and P based on the determined rate at which it is anticipated that the signals will be coupled through the bus.

30. (Previously Presented) The method of claim 17 wherein the acts of altering the values of N and P during the operation of the memory system comprise altering the values of N and P within a range of minimum and maximum values of N and P respectively.

31.-32. (Canceled)

33. (Previously Presented) The method of claim 17 wherein the act of coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus comprises transmitting a packet containing command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus.

34. (Previously Presented) The method of claim 17 wherein act of coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus comprises coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a uni-directional downstream bus having N signal lines, and wherein the

act of coupling data signals from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus comprises coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a uni-directional upstream bus having P signal lines.

35. (Original) The method of claim 17 wherein the acts of altering the values of N and P during the operation of the memory system comprise altering the values of N and P during the initialization of the memory system.

36. (Previously Presented) A memory system, comprising:

a memory hub controller having M buffers, N of the M buffers being configured as output buffers and P of the M buffers being configured as input buffers, the values of N and P being alterable during the operation of the memory system;

at least one memory module, comprising a memory hub having a plurality of buffers, N of which are configured as input buffers and P of which are configured as output buffers; and

a plurality of memory devices coupled to the memory hub; and

a bus having M signal lines each of which is coupled between a respective buffer of the memory hub controller and a respective buffer of the memory hub, the value of M being equal to the sum of N and P and the values of N and P further being altered within a range of minimum and maximum values of N and P respectively according to a rate of data transfer from the memory hub controller to the at least one memory module and a rate of data transfer from the at least one memory module to the memory hub controller such that the sum of N and P remains constant and equal to M by either transitioning at least one of the output buffers to input buffers or transitioning at least one of the input buffers to output buffers.

37.-38. (Canceled)

39. (Previously Presented) The memory system of claim 36 wherein the memory hub is operable to determine the rate at which the signals are being coupled through the bus, and wherein the values of M and N buffers for the respective buffers in the memory hub controller and the memory hub are altered based on the determined rate at which the signals are being coupled through the bus.

40. (Previously Presented) The memory system of claim 36 wherein the values of M and N buffers for the respective buffers in the memory hub controller and the memory hub are altered based on the rate at which the signals are being coupled through the bus from the memory hub controller to the memory hub.

41. (Previously Presented) The memory system of claim 36 wherein the values of M and N buffers for the respective buffers in the memory hub controller and the memory hub are altered based on the rate at which the signals are being coupled through the bus from the memory hub to the memory hub controller.

42. (Previously Presented) The memory system of claim 36 wherein the values of M and N buffers for the respective buffers in the memory hub controller and the memory hub are altered based on the rate at which it is anticipated that the signals will be coupled through the bus.

43. (Previously Presented) The memory system of claim 42 wherein the memory hub controller is operable to determine the rate at which it is anticipated that the signals will be coupled through the bus, and wherein the values of M and N buffers for the respective buffers in the memory hub controller and the memory hub are altered based on the determined rate at which it is anticipated that the signals will be coupled through the bus.

44. (Previously Presented) The memory system of claim 42 wherein the memory hub is operable to determine the rate at which it is anticipated that the signals will be coupled through the bus, and wherein the values of M and N buffers for the respective buffers in the memory hub controller and the memory hub are altered based on the determined rate at which it is anticipated that the signals will be coupled through the bus.

45. (Canceled)

46. (Original) The memory system of claim 36 wherein the memory hub controller is operable to alter the values of N and P during initialization of the memory system.

47. (Previously Presented) A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a peripheral device port;

a memory hub controller coupled to the processor bus, the memory hub controller having an output port and an input port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller;

at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub;

a downstream bus coupled between the output port of the memory controller and the memory hub of the at least one memory module, the downstream bus coupling first signals from the memory controller to the memory hub of the at least one memory module, the downstream bus having a width of M bits, the value of M being variable to adjust that bandwidth

of the downstream bus and the value of M further being alterable based on the rate at which the first signals are being coupled from the memory controller to the memory hub of the at least one memory module;

an upstream bus coupled between the input port of the memory controller and the memory hub of the at least one memory module, the upstream bus coupling second signals from the memory hub of the at least one memory module to the memory controller, the upstream bus having a width of N bits where N is equal to a fixed value less M, the value of N being variable to adjust that bandwidth of the upstream bus and the value of N further being alterable based on the rate at which the second signals are being coupled from the memory hub of the at least one memory module to the memory controller; and

wherein at least one of the memory hub controller and memory hub is operable to determine the rate at which the second and first signals are being coupled through the upstream and downstream buses, respectively, and wherein memory hub controller is operable to alter the values of M and N based on the determined rate by either transitioning at least one of the M bits of the downstream bus to one of the N bits of the upstream bus or transitioning at least one of the N bits of the upstream bus to one of the M bits of the downstream bus.

48.-49. (Canceled)

51. (Previously Presented) The processor-based system of claim 47 wherein the values of M and N are altered based on the rate at which the signals are being coupled through the downstream bus from the memory hub controller to the memory hub.

52. (Previously Presented) The processor-based system of claim 47 wherein the values of M and N are altered based on the rate at which the signals are being coupled through the upstream bus from the memory hub to the memory hub controller.

53. (Original) The processor-based system of claim 47 wherein the values of M and N are altered based on the rate at which it is anticipated that the signals will be coupled through at least one of the downstream bus and the upstream bus.

54. (Original) The processor-based system of claim 53 wherein the memory hub controller is operable to determine the rate at which it is anticipated that the signals will be coupled through at least one of the downstream bus and the upstream bus, and wherein the values of M and N are altered based on the determined rate at which it is anticipated that the signals will be coupled through at least one of the downstream bus and the upstream bus.

55. (Original) The processor-based system of claim 53 wherein the memory hub is operable to determine the rate at which it is anticipated that the signals will be coupled through at least one of the downstream bus and the upstream bus, and wherein the values of M and N are altered based on the determined rate at which it is anticipated that the signals will be coupled through at least one of the downstream bus and the upstream bus.

56. (Previously Presented) The processor-based system of claim 47 wherein the values of M and N are altered within a range of minimum and maximum values of M and N respectively.

57. (Previously Presented) The processor-based system of claim 47 wherein the values of M and N are altered during initialization of the processor-based system.

58. (Previously Presented) In a memory system having a memory hub controller and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, a method of coupling command, address and data signals between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a communications path having a first capacity;

coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a communications path having a second capacity, where the sum of the first capacity and the second capacity is a fixed value;

altering the first capacity and the second capacity during the operation of the memory system; and

configuring buffers in the memory hub controller and in the memory hub of the at least one memory module as either input buffers or output buffers;

wherein the acts of altering the first capacity and the second capacity comprise:

determining the rate at which it is anticipated that the signals will be coupled between the memory hub controller and the memory hub in the at least one memory module based on the type of hardware included in a system associated with the memory system; and

altering the first capacity and the second capacity based on the determined rate at which it is anticipated that the signals will be coupled between the memory hub controller and the memory hub in the at least one memory module by transitioning at least one of the output buffers to input buffers or transitioning at least one of the input buffers to output buffers.

59.-60. (Canceled)

61. (Previously Presented) The method of claim 58 wherein the acts of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity within a range of minimum and maximum values for the first capacity and the second capacity respectively.

62.-63. (Canceled)

64. (Previously Presented) The method of claim 58 wherein the act of coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module comprises transmitting a packet containing command, address and data signals from the memory hub controller to the memory hub in the at least one memory module.

65. (Previously Presented) The method of claim 58 wherein the acts of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity during the initialization of the memory system.

66. (Previously Presented) In a memory system having a memory hub controller and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, a method of coupling command, address and data signals between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a communications path having a first capacity and comprising a plurality of signal lines;

coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a communications path having a second capacity and comprising a plurality of signal lines, where the sum of the first capacity and the second capacity is a fixed value;

determining the rates at which it is anticipated that the command, address and data signals will be coupled from the memory hub controller to the memory hub in the at least one memory module and at which data signals will be coupled from the memory hub in the at least

one memory module to the memory hub controller based on the type of hardware included in a system associated with the memory system; and

altering the first capacity and the second capacity during the operation of the memory system based on the determined rate at which it is anticipated that the signals will be coupled from the memory hub controller to the memory hub in the at least one memory module and based on the rate at which it is anticipated that the signals will be coupled from the memory hub in the at least one memory module to the module memory hub controller by transitioning at least one of the plurality of signal lines from the first communications path to the second communications path or transitioning at least one of the plurality of signal lines from the second communications path to the first communications path.

67. (Previously Presented) The method of claim 66 wherein the acts of altering the first capacity and the second capacity comprise:

determining the rate at which it is anticipated that the signals will be coupled between the memory hub controller and the memory hub in the at least one memory module based on the type of hardware included in a system associated with the memory system; and

altering the first capacity and the second capacity based on the determined rate at which it is anticipated that the signals will be coupled between the memory hub controller and the memory hub in the at least one memory module.

68. (Previously Presented) The method of claim 66 wherein the acts of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity within a range of minimum and maximum values for the first capacity and the second capacity respectively.

69.-70. (Canceled)

71. (Previously Presented) The method of claim 66 wherein the act of coupling command, address and data signals from the memory hub controller to the memory hub

in the at least one memory module comprises transmitting a packet containing command, address and data signals from the memory hub controller to the memory hub in the at least one memory module.

72. (Previously Presented) The method of claim 66 wherein the acts of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity during the initialization of the memory system.

73. (Previously Presented) In a memory system having a memory hub controller and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, a method of coupling command, address and data signals between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a communications path having a first capacity and comprising a plurality of signal lines;

coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a communications path having a second capacity and comprising a plurality of signal lines, where the sum of the first capacity and the second capacity is a fixed value;

determining the rates at which the command, address and data signals are coupled from the memory hub controller to the memory hub and from the memory hub to the memory hub controller; and

altering the first capacity and the second capacity during the operation of the memory system according to the determined rates within a range of minimum and maximum values for the first capacity and the second capacity respectively by transitioning at least one of the plurality of signal lines from the first communications path to the second communications

path or transitioning at least one of the plurality of signal lines from the second communications path to the first communications path.

74.-75. (Canceled)

76. (Previously Presented) The method of claim 73 wherein the act of coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module comprises transmitting a packet containing command, address and data signals from the memory hub controller to the memory hub in the at least one memory module.

77. (Previously Presented) The method of claim 73 wherein the acts of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity during the initialization of the memory system.

78.-81. (Canceled)

82. (Previously Presented) In a memory system having a memory hub controller and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, a method of coupling command, address and data signals between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a communications path having a first capacity and comprising a plurality of signal lines;

coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a communications path having a second capacity and

comprising a plurality of signal lines, where the sum of the first capacity and the second capacity is a fixed value;

determining the rates at which the command, address and data signals are coupled from the memory hub controller to the memory hub and data signals are coupled from the memory hub to the memory hub controller; and

altering the first capacity and the second capacity during the operation of the memory system according to the determined rates by transitioning at least one of the plurality of signal lines from the first communications path to the second communications path or transitioning at least one of the plurality of signal lines from the second communications path to the first communications path.

83. (Previously Presented) The method of claim 82 wherein the acts of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity during the initialization of the memory system.

84. (Currently Amended) In a memory system having a memory hub controller, at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, and a bus having [[a]] M signal lines coupled between the memory hub controller and the memory hub in the at least one memory module, a method of coupling command, address and data signals through the bus between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus;

coupling data signals from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus, where N+P = M;

determining a first rate at which the command, address and data signals are coupled from the memory hub controller to the memory hub;

determining a second rate at which the data signals are coupled from the memory hub to the memory hub controller; and

altering the values of N and P during the operation of the memory system according to the first and second rates by transitioning buffers in the memory hub controller and in the memory hub of the at least one memory module from either input buffers to output buffers or output buffers to input buffers.

85. (Canceled)

86. (Previously Presented) The method of claim 84 wherein the acts of altering the values of N and P comprise:

determining the rate at which it is anticipated that the signals will be coupled through the bus; and

altering the values of N and P based on the determined rate at which it is anticipated that the signals will be coupled through the bus.

87. (Previously Presented) The method of claim 84 wherein the acts of altering the values of N and P during the operation of the memory system comprise altering the values of N and P within a range of minimum and maximum values of N and P respectively.

88.-89. (Canceled)

90. (Previously Presented) The method of claim 84 wherein the act of coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus comprises transmitting a packet containing command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus.

91. (Previously Presented) The method of claim 84 wherein act of coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus comprises coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a uni-directional downstream bus having N signal lines, and wherein the act of coupling data signals from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus comprises coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a uni-directional upstream bus having P signal lines.

92. (Previously Presented) The method of claim 84 wherein the acts of altering the values of N and P during the operation of the memory system comprise altering the values of N and P during the initialization of the memory system.

93. (Currently Amended) In a memory system having a memory hub controller, at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, and a bus having M signal lines coupled between the memory hub controller and the memory hub in the at least one memory module, a method of coupling command, address and data signals through the bus between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

coupling command, address and data signals in a downstream direction from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus;

coupling data signals in [[a]]an upstream direction from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus, where N+P = M;

determining a rate at which the command, address and data signals are coupled through the bus;

altering the values of N and P during the operation of the memory system based on the determined rate such that at least one of the M signal lines of the bus transitions from coupling in the upstream direction to coupling in the downstream direction or from coupling in the downstream direction to coupling in the upstream direction, the values of N and P being within a range of minimum and maximum values of N and P respectively.

94.-95. (Canceled)

96. (Previously Presented) The method of claim 93 wherein the act of coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus comprises transmitting a packet containing command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus.

97. (Previously Presented) The method of claim 93 wherein act of coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus comprises coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a uni-directional downstream bus having N signal lines, and wherein the act of coupling data signals from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus comprises coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a uni-directional upstream bus having P signal lines.

98. (Previously Presented) The method of claim 93 wherein the acts of altering the values of N and P during the operation of the memory system comprise altering the values of N and P during the initialization of the memory system.

99.-103. (Canceled)

104. (Currently Amended) In a memory system having a memory hub controller, at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, and a bus having [[a]]M signal lines coupled between the memory hub controller and the memory hub in the at least one memory module, a method of coupling command, address and data signals through the bus between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

coupling command, address and data signals in a downstream direction from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus;

coupling data signals in [[a]]an upstream direction from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus, where N+P = M;

determining a rate during operation at which the command, address and data signals coupled from the memory hub controller to the memory hub and data signals coupled from the memory hub in the at least one memory module to the memory controller are coupled through the bus; and

altering the values of N and P during the operation of the memory system based on the determined rate such that at least one of the M signal lines of the bus transitions from coupling in the upstream direction to coupling in the downstream direction or from coupling in the downstream direction to coupling in the upstream direction.

105. (Previously Presented) The method of claim 104 wherein act of coupling signals in a packet that includes command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus comprises coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a uni-directional downstream bus having N signal lines, and wherein the act of coupling data signals from the memory hub in the

at least one memory module to the memory hub controller using P of the M signal lines of the bus comprises coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a uni-directional upstream bus having P signal lines.

106. (Previously Presented) The method of claim 104 wherein the acts of altering the values of N and P during the operation of the memory system comprise altering the values of N and P during the initialization of the memory system.

107. (Currently Amended) In a memory system having a memory hub controller, at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, and a bus having [[a]] M signal lines coupled between the memory hub controller and the memory hub in the at least one memory module, a method of coupling command, address and data signals through the bus between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

coupling command, address and data signals in a downstream direction from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus and further using a uni-directional downstream bus having N signal lines;

coupling data signals in [[a]]an upstream direction from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus and further using a uni-directional upstream bus having P signal lines, where N+P = M;

determining the rates during operation at which the command, address and data signals are coupled from the memory hub controller to the memory hub and at which data signals are coupled from the memory hub to the memory hub controller; and

altering the values of N and P during the operation of the memory system according to the determined rates such that at least one of the M signal lines of the bus transitions from coupling in the upstream direction to coupling in the downstream direction or from coupling in the downstream direction to coupling in the upstream direction.

108. (Previously Presented) The method of claim 107 wherein the acts of altering the values of N and P during the operation of the memory system comprise altering the values of N and P during the initialization of the memory system.

109. (Previously Presented) A memory system, comprising:

a memory hub controller having M buffers, N of the M buffers being configured as output buffers and P of the M buffers being configured as input buffers, the values of N and P being alterable during initialization of the memory system;

at least one memory module, comprising a memory hub having a plurality of buffers, N of which are configured as input buffers and P of which are configured as output buffers; and

a plurality of memory devices coupled to the memory hub; and

a bus having M signal lines each of which is coupled between a respective buffer of the memory hub controller and a respective buffer of the memory hub, the value of M being equal to the sum of N and P; and

wherein at least one of the memory hub and memory hub controller is operable to determine the rate at which signals are being coupled through the bus, and wherein the values of P and N buffers for the respective buffers in the memory hub controller and the memory hub are altered based on the determined rate at which the signals are being coupled through the bus by transitioning at least one of the input buffers to output buffers or at least one of the output buffers to input buffers.

110. (Previously Presented) The memory system of claim 109 wherein the values of M and N buffers for the respective buffers in the memory hub controller and the memory hub-are altered based on the rate at which the signals are being coupled through the bus.

111. (Previously Presented) The memory system of claim 110 wherein the memory hub controller is operable to determine the rate at which the signals are being coupled through the bus, and wherein the values of M and N buffers for the respective buffers in the

memory hub controller and the memory hub are altered based on the determined rate at which the signals are being coupled through the bus.

112. (Previously Presented) The memory system of claim 110 wherein the memory hub is operable to determine the rate at which the signals are being coupled through the bus, and wherein the values of M and N buffers for the respective buffers in the memory hub controller and the memory hub are altered based on the determined rate at which the signals are being coupled through the bus.

113. (Previously Presented) The memory system of claim 110 wherein the values of M and N buffers for the respective buffers in the memory hub controller and the memory hub are altered based on the rate at which the signals are being coupled through the bus from the memory hub controller to the memory hub.

114. (Previously Presented) The memory system of claim 110 wherein the values of M and N buffers for the respective buffers in the memory hub controller and the memory hub are altered based on the rate at which the signals are being coupled through the bus from the memory hub to the memory hub controller.

115. (Previously Presented) The memory system of claim 109 wherein the values of M and N buffers for the respective buffers in the memory hub controller and the memory hub are altered based on the rate at which it is anticipated that the signals will be coupled through the bus.

116. (Previously Presented) The memory system of claim 115 wherein the memory hub controller is operable to determine the rate at which it is anticipated that the signals will be coupled through the bus, and wherein the values of M and N buffers for the respective buffers in the memory hub controller and the memory hub are altered based on the determined rate at which it is anticipated that the signals will be coupled through the bus.

117. (Previously Presented) The memory system of claim 115 wherein the memory hub is operable to determine the rate at which it is anticipated that the signals will be coupled through the bus, and wherein the values of M and N buffers for the respective buffers in the memory hub controller and the memory hub are altered based on the determined rate at which it is anticipated that the signals will be coupled through the bus.

118. (Previously Presented) A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a peripheral device port;

a memory hub controller coupled to the processor bus, the memory hub controller having an output port and an input port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller;

at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub;

a downstream bus coupled between the output port of the memory controller and the memory hub of the at least one memory module, the downstream bus having a width of M bits, the value of M being variable to adjust that bandwidth of the downstream bus and the value of M further being alterable based on the rate at which it is anticipated that the signals will be coupled through at least the downstream bus; and

an upstream bus coupled between the input port of the memory controller and the memory hub of the at least one memory module, the upstream bus having a width of N bits where N is equal to a fixed value less M, the value of N being variable to adjust that bandwidth

of the upstream bus and the value of N further being alterable based on the rate at which it is anticipated that the signals will be coupled through at least the upstream bus;

wherein at least one of the memory hub controller and the memory hub of the at least one controller operable to

determine the rate at which it is anticipated that the signals will be coupled between the memory hub controller and the memory hub in the at least one memory module based on the type of hardware included in a system associated with the memory system; and

alter the values of M and N based on the determined rates at which it is anticipated that the signals will be coupled between the memory hub controller and the memory hub in the at least one memory module by transitioning at least one of the M bits of the downstream bus to the upstream bus or transitioning at least one of the N bits of the upstream bus to the downstream bus.

119.-120. (Canceled)

121. (Previously Presented) The processor-based system of claim 118 wherein the values of M and N are altered within a range of minimum and maximum values of M and N respectively.

122. (Previously Presented) The processor-based system of claim 118 wherein the values of M and N are altered during initialization of the processor-based system.